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S3C2440A

32-位 CMOS

微型控制器

用户手册

修订版本 1

第一章产品概述

--------马志晶译

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1 产品概述

引言

三星公司推出的16/32位RISC微处理器S3C2440A，为手持设备和一般类型应用提供了低价格、低功耗、高性能小型微控制器的解决方案。

为了降低整体系统成本，S3C2440A 提供了一下丰富的内部设备

S3C2440A 采用了 ARM920t 的内核，0.13um 的 CMOS 标准宏单元和存储器单元。其低功耗，简单，优雅，且全静态设计特别适合于对成本和功率敏感型的应用。它采用了新的总线架构 Advanced Micro controller Bus Architecture (AMBA). 。

S3C2440A 的杰出的特点是其核心处理器(CPU)，是一个由 Advanced RISC Machines 有限公司设计的 16/32 位 ARM920T 的 RISC 处理器。ARM920T 实现了 MMU， AMBA BUS 和 Harvard 高速缓冲体系结构构。这一结构具有独立的 16KB 指令 Cache 和 16KB 数据 Cache。每个都是由具有 8 字长的行组成。通过提供一套完整的通用系统外设， S3C2440A 减少整体系统成本和无需配置额外的组件。

综合对芯片的功能描述，本手册将介绍 S3C2440A 集成的以下片上功能：

- 1.2V 内核供电, 1.8V/2.5V/3.3V存储器供电，3.3V 外部I/O供电 具备16KB的 I-Cache和16KB DCache/MMU微处理器
- 外部存储控制器(SDRAM 控制和片选逻辑)
- LCD 控制器（最大支持4K 色STN 和256K 色TFT）提供1 通道LCD 专用DMA。
- 4 通道DMA 并有外部请求引脚。
- 3 通道UART(IrDA1.0, 64字节Tx FIFO，和64字节Rx FIFO)
- 2 通道SPI
- 1 通道IIC-BUS接口（多主支持）
- 1通道IIS-BUS音频编解码器接口
- AC'97 解码器接口
- 兼容SD 主接口协议1.0 版和MMC 卡协议2.11 兼容版。
- 2 端口USB 主机/1 端口USB 设备（1.1 版）
- 4 通道PWM 定时器和 1 通道内部定时器 / 看门狗定时器
- 8 通道10 比特ADC 和触摸屏接口
- 具有日历功能的RTC
- 相机接口（最大4096 × 4096像素的投入支持。 2048 × 2048像素的投入，支持缩放）
- 130 个通用I/O 口和24 通道外部中断源。
- 具有普通，慢速，空闲和掉电模式。
- 具有PLL 片上时钟发生器

特性

体系结构

- 为手持设备和通用嵌入式应用提供片上集成系统解决方案.
- 16/32 位RISC 体系结构和ARM920T 内核强大的指令集

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- 加强的ARM 体系结构MMU 用于支持WinCE,EPOC 32 和Linux.
- 指令高速存储缓冲器（I-Cache），数据高速存储缓冲器（D-Cache），写缓冲器和物理地址TAG RAM 减少主存带宽和响应性带来的影响.
- 采用ARM920T CPU 内核支持ARM 调试体系结构.
- 内部高级微控制总线（AMBA）体系结构(AMBA2.0，AHB/APB).

系统管理器

- 支持大/小端方式.
- 支持高速总线模式和异步总线模式.
- 寻址空间：每bank 128M 字节（总共1G 字节）.
- 支持可编程的每bank 8/16/32 位数据总线带宽.
- 从bank 0 到bank 6 都采用固定的bank 起始寻址.
- bank7 具有可编程的bank 的起始地址和大小
- 8 个存储器bank：

－其中6 个适用于ROM,SRAM,和其他

－另外2 个适用于ROM/SRAM 和同步DRAM.

- 所有的存储器bank 都具有可编程的操作周期.
- 支持外部等待信号延长总线周期.
- 支持掉电时的SDRAM 自刷新模式.
- 支持各种型号的ROM 引导（NOR/NAND Flash，EEPROM，或其他）.

NAND Flash 启动引导

- 支持从NAND flash 存储器的启动.
- 采用4KB 内部缓冲器进行启动引导.
- 支持启动之后NAND 存储器仍然作为外部存储器使用.
- 支持先进的 NAND flash

Cache 存储器

- 64 项全相连模式，采用I-Cache(16KB)和D-Cache(16KB.
- 每行8 字长度，其中每行带有一个有效为和两个dirty 位.
- 伪随机数或轮转循环替换算法.
- 采用写穿式（write-through）或写回式（write-back）cache 操作来更新主存储器.
- 写缓冲器可以保存16 个字的数据和4 个地址.

时钟和电源管理

- 片上MPLL 和UPLL:

  采用UPLL 产生操作USB 主机/设备的时钟

  MPLL 产生最大400MHZ@ 1.3V操作MCU 所需要的时钟
- 通过软件可以有选择性的为每个功能模块提供时钟.
- 电源模式：正常，慢速，空闲和掉电模式

  正常模式：正常运行模式

  慢速模式：不加PLL 的低时钟频率模式.

  空闲模式：只停止CPU 的时钟；

  掉电模式：所有外设和内核的电源都切断了；
- 可以通过EINT[15:0]或RTC 报警中断来从掉电模式中唤醒处理器

特点（续）

中断控制器

- 60 个中断源（1 个看门狗定时器，5 个定时器，9 个UARTs，24 个外部中断，4 个DMA,2

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个RTC,2 个ADC,1 个IIC,2 个SPI,1 个SDI,2 个USB,1 个LCD,和1 个电池故障，1个NAND 和 2 个Camera), 1 AC97音频

- 电平/边沿触发模式的外部中断源
- 可编程的边沿/电平触发极性
- 支持为紧急中断请求提供快速中断服务

具有脉冲带宽调制功能的定时器 (PWM)

- 4 通道16 位具有PWM 功能的定时器，1 通道16 位内部定时器，可基于DMA 或中断工作
- 可编程的占空比周期，频率和极性
- 能产生死区
- 支持外部时钟源

RTC（实时时钟）

- 全面的时钟特性：秒、分、时、日期，星期，月和年；
- 32.768KHz 工作
- 具有报警中断
- 具有节拍中断

通用I/O 端口

- 24 个外部中断端口
- 130 个多功能输入/输出端口

DMA 控制器

- 4 通道的DMA 控制器；
- 支持存储器到存储器，IO 到存储器，存储器到IO 和IO 到IO 的传输s
- 采用触发传输模式来加快传输速率

LCD 控制器STN LCD 显示特性

- 支持3 种类型的STN LCD 显示屏：4 位双扫描，4 位单扫描，8 位单扫描显示类型
- 支持单色模式、4 级、16 级灰度STN LCD、256 色和4096 色STN LCD
- 支持多种不同尺寸的液晶屏

–LCD 实际尺寸的典型值是：640×480，320×240，160×160 及其他.

–最大虚拟屏幕大小是4M 字节.

–256 色模式下支持的最大虚拟屏是：4096×1024，2048×2048，1024×4096 等

TFT 彩色显示屏

- 支持彩色TFT 的1，2，4 或8bbp(像素每位)调色显示
- 支持16，24bbp 无调色真彩显示 TFT
- 在24bbp 模式下支持最大16M 色TFT
- lpc3600定时控制器，为嵌入式lts350Q1-PD1/2 （SAMSUNG 3.5" Portrait/256kcolor/ 一Reflective a-Si TFT LCD）
- lpc3600定时控制器，为嵌入式lts350Q1-PE1/2 （SAMSUNG 3.5” Portrait / 256Kcolor/ Transflective a-Si TFT LCD）

支持多种不同尺寸的液晶屏

–典型实屏尺寸：640×480，320×240，160×160 及其他

–最大虚拟屏大小4M 字节.

–64K 色彩模式下最大的虚拟屏尺寸为2048×1024 及其他

UART

- 3 通道UART，可以基于DMA 模式或中断模式工作

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- 支持5 位，6 位，7 位或者8 位串行数据发送/接收
- 支持外部时钟作为UART 的运行时钟（UEXTCLK）
- 可编程的波特率
- 支持IrDA1.0
- 具有测试用的还回模式
- 每个通道都具有内部64 字节的发送FIFO 和64 字节的接收FIFO.

特点（续）

A/D 转换和触摸屏接口

- 8 通道多路复用ADC
- 最大500KSPS/10 位精度
- 内部TFT 直接触摸屏接口

看门狗定时器

- 16 位看门狗定时器
- 在定时器溢出时发生中断请求或系统复位

IIC 总线接口

- 1 通道多主IIC 总线
- 可进行串行，8 位，双向数据传输，标准模式下数据传输速度可达100kbit/s，快速模式下可达到400kbit/s.

IIS 总线接口

- 1 通道音频IIS 总线接口，可基于DMA 方式工作
- 串行，每通道8/16 位数据传输
- 发送和接收具备128 字节(64 字节加64 字节)FIFO
- 支持IIS 格式和MSB-justified 数据格式

AC97 音频解码器接口

- 支援16位采样
- 1-ch 立体声 PCM 输入/ 1-ch 立体声 PCM 输出1-ch MIC 输入

USB 主设备

- 2 个 USB 主设备接口
- 遵从OHCI Rev.1.0 标准
- 遵从OHCI Rev.1.0 标准

USB 从设备

- 1 个USB 从设备接口
- 具备5 个Endpoint
- 兼容USB ver1.1 标准

SD 主机接口

- 正常，中断和dma数据传输模式（字节， 半字节 ， 文字传递）
- DMA burst4接入支持（只字转让）
- 兼容SD 存储卡协议1.0 版
- 兼容SDIO 卡协议1.0 版
- 发送和接收具有64字节FIFO
- 兼容MMC 卡协议2.11 版

SPI 接口

- 兼容2 通道SPI 协议2.11 版

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- 发送和接收具有2×8 位的移位寄存器
- 可以基于DMA 或中断模式工作

相机接口

- 支持 ITU-R BT 601/656 8-bit 模式
- 具有DZI (数字变焦) 能力
- 具有极性可编程视频同步信号
- 最大值支持. 4096 x 4096 像素输入(支持 2048 × 2048像素输入缩放)
- 镜头旋转 (x轴， y轴，和180 °旋转)
- 相机输出格式（ 16/24-bit的RGB与YCBCR 4:2:0/4:2:2格式）

工作电压

- 内核： 300MHz 时 1.20V
  400MHz 时 1.3V

内存：支持1.8v / 2.5v/3.0v/3.3v

- 输入/输出：3.3v

操作频率

- Fclk 最高达 400MHz
- Hclk 最高达 136MHz
- Pclk 最高达 68MHz

封装

- 289-FBGA

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内部结构图

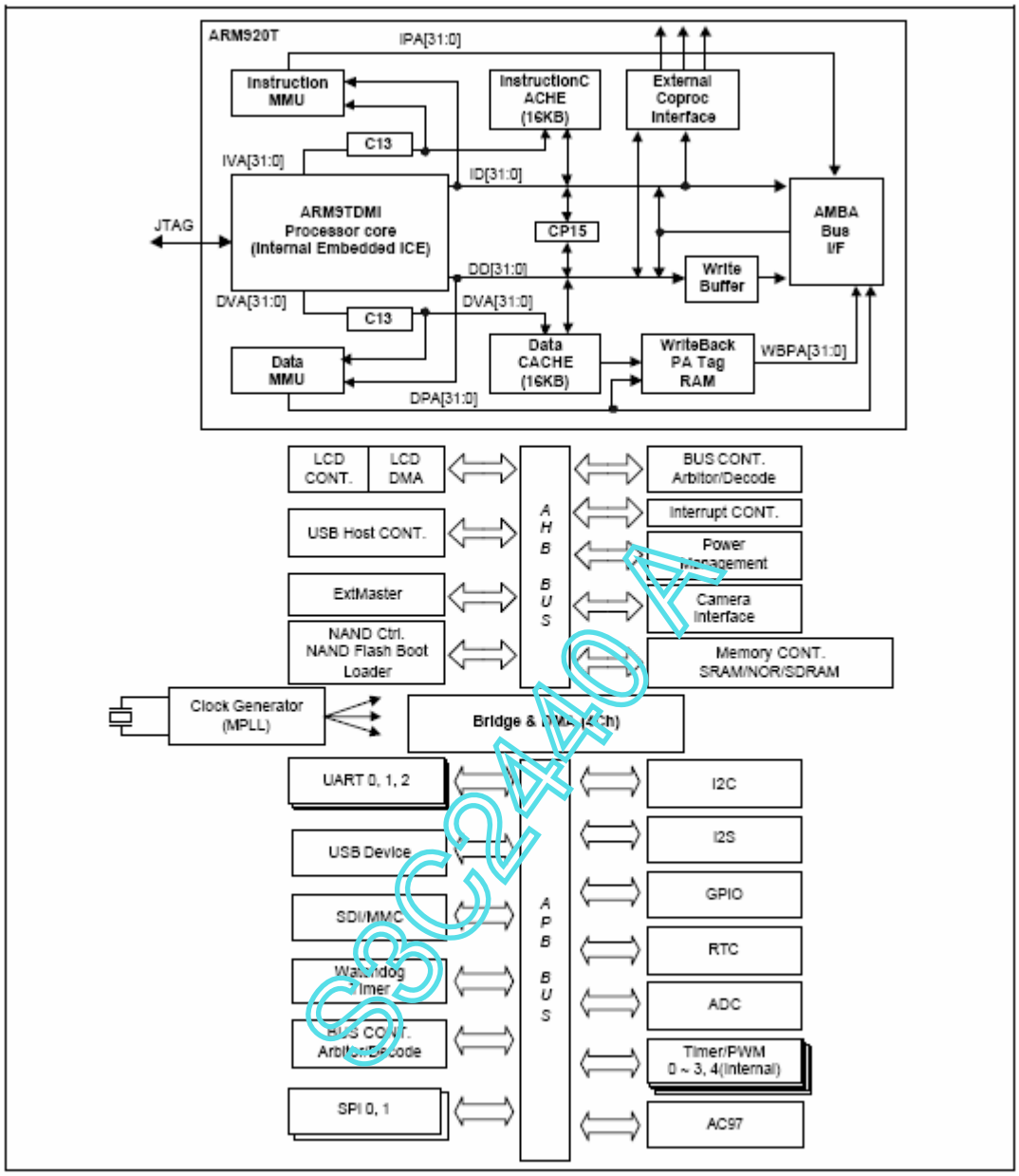

Figure 1-1. S3C2440A Block Diagram

图 1-1. S3C2440A 方框图

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管脚分配

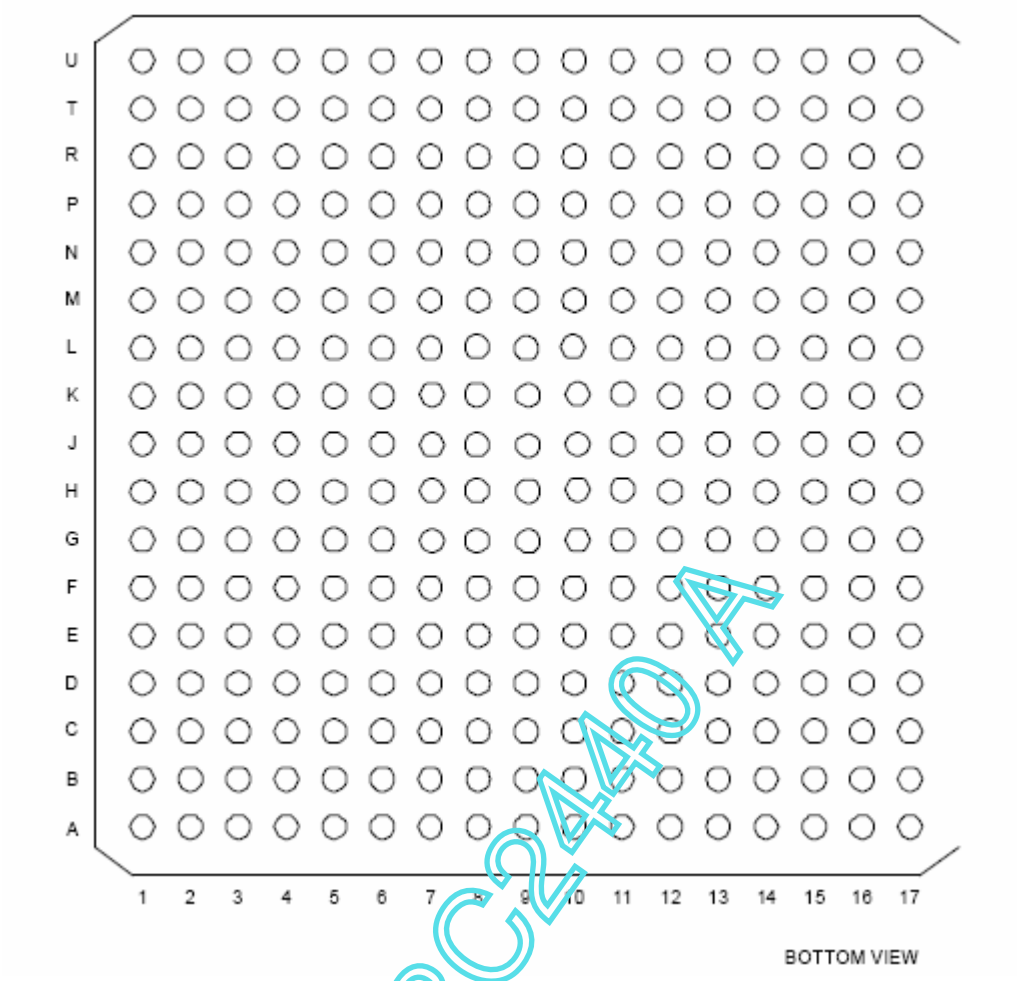

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图1-2. S3C2440A引脚定义图(289-FBGA)

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表 1-1 。 289 针脚 fbga 的管脚分配-密码命令（表 1 3 ）

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	VDDi	C1	VDDMOP	E1	nFRE/GPA20
A2	SCKE	C2	nGCS5/GPA16	E2	VSSMOP
A3	VSSi	C3	nGCS2/GPA13	E3	nGCS7
A4	VSSi	C4	nGCS3/GPA14	E4	nWAIT
A5	VSSMOP	C5	nOE	E5	nBE3
A6	VDDi	C6	nSRAS	E6	nWE
A7	VSSMOP	C7	ADDR4	E7	ADDR1
A8	ADDR10	C8	ADDR11	E8	ADDR6
A9	VDDMOP	C9	ADDR15	E9	ADDR14
A10	VDDi	C10	ADDR21/GPA6	E10	ADDR23/GPA8
A11	VSSMOP	C11	ADDR24/GPA9	E11	DATA2
A12	VSSi	C12	DATA1	E12	DATA20
A13	DATA3	C13	DATA6	E13	DATA19
A14	DATA7	C14	DATA11	E14	DATA18
A15	VSSMOP	C15	DATA13	E15	DATA17
A16	VDDi	C16	DATA16	E16	DATA21
A17	DATA10	C17	VSSi	E17	DATA24
B1	VSSMOP	D1	ALE/GPA18	F1	VDDi
B2	nGCS1/GPA12	D2	nGCS6	F2	VSSi
B3	SCLK1	D3	nGCS4/GPA15	F3	nFWE/GPA19
B4	SCLK0	D4	nBE0	F4	nFCE/GPA22
B5	nBE1	D5	nBE2	F5	CLE/GPA17
B6	VDDMOP	D6	nSCAS	F6	nGCS0
B7	ADDR2	D7	ADDR7	F7	ADDR0/GPA0
B8	ADDR9	D8	ADDR5	F8	ADDR3
B9	ADDR12	D9	ADDR16/GPA1	F9	ADDR18/GPA3
B10	VSSi	D10	ADDR20/GPA5	F10	DATA4
B11	VDDi	D11	ADDR26/GPA11	F11	DATA5
B12	VDDMOP	D12	DATA0	F12	DATA27
B13	VSSMOP	D13	DATA8	F13	DATA31
B14	VDDMOP	D14	DATA14	F14	DATA26
B15	DATA9	D15	DATA12	F15	DATA22
B16	VDDMOP	D16	VSSMOP	F16	VDDi
B17	DATA15	D17	VSSMOP	F17	VDDMOP

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表 1-1 。 289 针脚 fbga 的管脚分配-密码令（第 2 页共 3 页） （续）

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
G1	VSSOP	J1	VDDOP	L1	LEND/GPC0
G2	CAMHREF/GPJ10	J2	VDDiarm	L2	VDDiarm
G3	CAMDATA1/GPJ1	J3	CAMCLKOUT/GPJ11	L3	nXDACK0/GPB9
G4	VDDalive	J4	CAMRESET/GPJ12	L4	VCLK/GPC1
G5	CAMPCLK/GPJ8	J5	TOUT1/GPB1	L5	nXBREQ/GPB6
G6	FRnB	J6	TOUT0/GPB0	L6	VD1/GPC9
G7	CAMVSYNC/GPJ9	J7	TOUT2/GPB2	L7	VFRAME/GPC3
G8	ADDR8	J8	CAMDATA6/GPJ6	L8	I2SSDI/AC_SDATA_IN
G9	ADDR17/GPA2	J9	SDDAT3/GPE10	L9	SPICLK0/GPE13
G10	ADDR25/GPA10	J10	EINT10/nSS0/GPG2	L10	EINT15/SPICLK1/GPG7
G11	DATA28	J11	TXD2/nRTS1/GPH6	L11	EINT22/GPG14
G12	DATA25	J12	PWREN	L12	Xtortc
G13	DATA23	J13	TCK	L13	EINT2/GPF2
G14	XTIpll	J14	TMS	L14	EINT5/GPF5
G15	XTOpll	J15	RXD2/nCTS1/GPH7	L15	EINT6/GPF6
G16	DATA29	J16	TDO	L16	EINT7/GPF7
G17	VSSi	J17	VDDalive	L17	nRTS0/GPH1
H1	VSSiarm	K1	VSSiarm	M1	VLINE/GPC2
H2	CAMDATA7/GPJ7	K2	nXDACK1/GPB5	M2	LCD_LPCREV/GPC6
H3	CAMDATA4/GPJ4	K3	TOUT3/GPB3	M3	LCD_LPCOE/GPC5
H4	CAMDATA3/GPJ3	K4	TCLK0/GPB4	M4	VM/GPC4
H5	CAMDATA2/GPJ2	K5	nXDREQ1/GPB8	M5	VD9/GPD1
H6	CAMDATA0/GPJ0	K6	nXDREQ0/GPB10	M6	VD8/GPC14
H7	CAMDATA5/GPJ5	K7	nXDACK1/GPB7	M7	VD16/SPIMISO1/GPD8
H8	ADDR13	K8	SDCMD/GPE6	M8	SDDAT1/GPE8
H9	ADDR19/GPA4	K9	SPIMISO0/GPE11	M9	IICSDA/GPE15
H10	ADDR22/GPA7	K10	EINT13/SPIMISO1/GPG5	M10	EINT20/GPG12
H11	VSSOP	K11	nCTS0/GPH0	M11	EINT17/nRTS1/GPG9
H12	EXTCLK	K12	VDDOP	M12	VSSA_UPLL
H13	DATA30	K13	TXD0/GPH2	M13	VDDA_UPLL
H14	nBATT_FLT	K14	RXD0/GPH3	M14	Xtirtc
H15	nTRST	K15	UEXTCLK/GPH8	M15	EINT3/GPF3
H16	nRESET	K16	TXD1/GPH4	M16	EINT1/GPF1
H17	TDI	K17	RXD1/GPH5	M17	EINT4/GPF4

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表 1-1 。 289 针脚 fbga 的管脚分配-密码顺序（表 3 ） （续）

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
N1	VSSOP	P15	AIN3	T12	VDDOP
N2	VD0/GPC8	P16	XP/AIN7	T13	OM3
N3	VD4/GPC12	P17	UPLLCAP	T14	VSSA_ADC
N4	VD2/GPC10	R1	VD3/GPC11	T15	OM0
N5	VD10/GPD2	R2	VD8/GPD0	T16	YM/AIN4
N6	VD15/GPD7	R3	VD11/GPD3	T17	YP/AIN5
N7	VD22/nSS1/GPD14	R4	VD13/GPD5	U1	VDDiarm
N8	SDCLK/GPE5	R5	VD18/SPICLK1/GPD10	U2	VDDiarm
N9	EINT8/GPG0	R6	VD21 /GPD13	U3	VSSOP
N10	EINT18/nCTS1/GPG10	R7	I2SSCLK/AC_BIT_CLK	U4	VSSiarm
N11	DP0	R8	SDDAT0/GPE7	U5	VD23/nSS0/GPD15
N12	DN1/PDN0	R9	CLKOUT0/GPH9	U6	I2SSDO/AC_SDATA_ OUT
N13	nRSTOUT/GPA21	R10	EINT11/nSS1/GPG3	U7	VSSiarm
N14	MPLLCAP	R11	EINT14/SPIMOSI1/GPG6	U8	IICSCL/GPE14
N15	VDD_RTC	R12	NCON	U9	VSSOP
N16	VDDA_MPLL	R13	OM1	U10	VSSiarm
N17	EINT0/GPF0	R14	AIN0	U11	VDDi
P1	LCD_LPCREVB/GPC7	R15	AIN2	U12	EINT19/TCLK1/GPG11
P2	VD5/GPC13	R16	XM/AIN6	U13	EINT23/GPG15
P3	VD7/GPC15	R17	VSSA_UPLL	U14	DP1/PDP0
P4	VD12/GPD4	T1	VSSiarm	U15	VSSOP
P5	VD14/GPD6	T2	VSSiarm	U16	Vref
P6	VD20/GPD12	T3	VDDOP	U17	AIN1
P7	I2SLRCK/AC_SYNC	T4	VD17/SPIMOSI1/GPD9		
P8	SDDAT2/GPE9	T5	VD19/GPD11		
P9	SPIMOSI0/GPE12	T6	VDDiarm		
P10	CLKOUT1/GPH10	T7	CDCLK/AC_nRESET		
P11	EINT12/LCD_PWREN/ GPG4	T8	VDDiarm		
P12	DN0	T9	EINT9/GPG1		
P13	OM2	T10	EINT16/GPG8		
P14	VDDA_ADC	T11	EINT21/GPG13		

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表 1-2 。 s3c2440a 289 引脚 fbga 的管脚分配（表 1/9）

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
F7	ADDR0/GPA0	ADDR0	Hi-z/–	O(L)/–	O(L)	t10s
E7	ADDR1	ADDR1	Hi-z	O(L)	O(L)	t10s
B7	ADDR2	ADDR2	Hi-z	O(L)	O(L)	t10s
F8	ADDR3	ADDR3	Hi-z	O(L)	O(L)	t10s
C7	ADDR4	ADDR4	Hi-z	O(L)	O(L)	t10s
D8	ADDR5	ADDR5	Hi-z	O(L)	O(L)	t10s
E8	ADDR6	ADDR6	Hi-z	O(L)	O(L)	t10s
D7	ADDR7	ADDR7	Hi-z	O(L)	O(L)	t10s
G8	ADDR8	ADDR8	Hi-z	O(L)	O(L)	t10s
B8	ADDR9	ADDR9	Hi-z	O(L)	O(L)	t10s
A8	ADDR10	ADDR10	Hi-z	O(L)	O(L)	t10s
C8	ADDR11	ADDR11	Hi-z	O(L)	O(L)	t10s
B9	ADDR12	ADDR12	Hi-z	O(L)	O(L)	t10s
H8	ADDR13	ADDR13	Hi-z	O(L)	O(L)	t10s
E9	ADDR14	ADDR14	Hi-z	O(L)	O(L)	t10s
C9	ADDR15	ADDR15	Hi-z	O(L)	O(L)	t10s
D9	ADDR16/GPA1	ADDR16	Hi-z/–	O(L)/–	O(L)	t10s
G9	ADDR17/GPA2	ADDR17	Hi-z/–	O(L)/–	O(L)	t10s
F9	ADDR18/GPA3	ADDR18	Hi-z/–	O(L)/–	O(L)	t10s
H9	ADDR19/GPA4	ADDR19	Hi-z/–	O(L)/–	O(L)	t10s
D10	ADDR20/GPA5	ADDR20	Hi-z/–	O(L)/–	O(L)	t10s
C10	ADDR21/GPA6	ADDR21	Hi-z/–	O(L)/–	O(L)	t10s
H10	ADDR22/GPA7	ADDR22	Hi-z/–	O(L)/–	O(L)	t10s
E10	ADDR23/GPA8	ADDR23	Hi-z/–	O(L)/–	O(L)	t10s
C11	ADDR24/GPA9	ADDR24	Hi-z/–	O(L)/–	O(L)	t10s
G10	ADDR25/GPA10	ADDR25	Hi-z/–	O(L)/–	O(L)	t10s
D11	ADDR26/GPA11	ADDR26	Hi-z/–	O(L)/–	O(L)	t10s
R14	AIN0	AIN0	–	–	AI	r10
U17	AIN1	AIN1	–	–	AI	r10
R15	AIN2	AIN2	–	–	AI	r10
P15	AIN3	AIN3	–	–	AI	r10
T16	YM/AIN4	AIN4	–/–	–/–	AI	r10
T17	YP/AIN5	YP	–/–	–/–	AI	r10
R16	XM/AIN6	AIN6	–/–	–/–	AI	r10

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表 1-2 。 s3c2440a 289 引脚 fbga 的管脚分配（表 2/9） （续） ）

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
P16	XP/AIN7	XP	–/–	–/–	AI	r10
H8	CAMDATA0/GPJ0	GPJ0	–/–	Hi-z/–	I	t8
G3	CAMDATA1/GPJ1	GPJ1	–/–	Hi-z/–	I	t8
H5	CAMDATA2/GPJ2	GPJ2	–/–	Hi-z/–	I	t8
H4	CAMDATA3/GPJ3	GPJ3	–/–	Hi-z/–	I	t8
H3	CAMDATA4/GPJ4	GPJ4	–/–	Hi-z/–	I	t8
H7	CAMDATA5/GPJ5	GPJ5	–/–	Hi-z/–	I	t8
J8	CAMDATA6/GPJ6	GPJ6	–/–	Hi-z/–	I	t8
H2	CAMDATA7/GPJ7	GPJ7	–/–	Hi-z/–	I	t8
G5	CAMPCLK/GPJ8	GPJ8	–/–	Hi-z/–	I	t8
G7	CAMVSYNC/GPJ9	GPJ9	–/–	Hi-z/–	I	t8
G2	CAMHREF/GPJ10	GPJ10	–/–	Hi-z/–	I	t8
J3	CAMCLKOUT/GPJ11	GPJ11	–/–	O(L)/–	I	t8
J4	CAMRESET/GPJ12	GPJ12	–/–	O(L)/–	I	t8
D12	DATA0	DATA0	Hi-z	Hi-z/O(L)	I	b12s
C12	DATA1	DATA1	Hi-z	Hi-z,O(L)	I	b12s
E11	DATA2	DATA2	Hi-z	Hi-z,O(L)	I	b12s
A13	DATA3	DATA3	Hi-z	Hi-z,O(L)	I	b12s
F10	DATA4	DATA4	Hi-z	Hi-z,O(L)	I	b12s
F11	DATA5	DATA5	Hi-z	Hi-z,O(L)	I	b12s
C13	DATA6	DATA6	Hi-z	Hi-z,O(L)	I	b12s
A14	DATA7	DATA7	Hi-z	Hi-z,O(L)	I	b12s
D13	DATA8	DATA8	Hi-z	Hi-z,O(L)	I	b12s
B15	DATA9	DATA9	Hi-z	Hi-z,O(L)	I	b12s
A17	DATA10	DATA10	Hi-z	Hi-z,O(L)	I	b12s
C14	DATA11	DATA11	Hi-z	Hi-z,O(L)	I	b12s
D15	DATA12	DATA12	Hi-z	Hi-z,O(L)	I	b12s
C15	DATA13	DATA13	Hi-z	Hi-z,O(L)	I	b12s
D14	DATA14	DATA14	Hi-z	Hi-z,O(L)	I	b12s
B17	DATA15	DATA15	Hi-z	Hi-z,O(L)	I	b12s
C16	DATA16	DATA16	Hi-z	Hi-z,O(L)	I	b12s
E15	DATA17	DATA17	Hi-z	Hi-z,O(L)	I	b12s
E14	DATA18	DATA18	Hi-z	Hi-z,O(L)	I	b12s

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表 1-2 。 s3c2440a 289 引脚 fbga 的管脚分配（表 3/9） （续） ）

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
E13	DATA19	DATA19	Hi-z	Hi-z,O(L)	I	b12s
E12	DATA20	DATA20	Hi-z	Hi-z,O(L)	I	b12s
E16	DATA21	DATA21	Hi-z	Hi-z,O(L)	I	b12s
F15	DATA22	DATA22	Hi-z	Hi-z,O(L)	I	b12s
G13	DATA23	DATA23	Hi-z	Hi-z,O(L)	I	b12s
E17	DATA24	DATA24	Hi-z	Hi-z,O(L)	I	b12s
G12	DATA25	DATA25	Hi-z	Hi-z,O(L)	I	b12s
F14	DATA26	DATA26	Hi-z	Hi-z,O(L)	I	b12s
F12	DATA27	DATA27	Hi-z	Hi-z,O(L)	I	b12s
G11	DATA28	DATA28	Hi-z	Hi-z,O(L)	I	b12s
G16	DATA29	DATA29	Hi-z	Hi-z,O(L)	I	b12s
H13	DATA30	DATA30	Hi-z	Hi-z,O(L)	I	b12s
F13	DATA31	DATA31	Hi-z	Hi-z,O(L)	I	b12s
P12	DN0	DN0	–	–	AI	us
N11	DP0	DP0	–	–	AI	us
N12	DN1/PDN0	DN1	–/–	–	AI	us
U14	DP1/PDP0	DP1	–/–	–	AI	us
N17	EINT0/GPF0	GPF0	–/–	Hi-z/–	I	t8
M16	EINT1/GPF1	GPF1	–/–	Hi-z/–	I	t8
L13	EINT2/GPF2	GPF2	–/–	Hi-z/–	I	t8
M15	EINT3/GPF3	GPF3	–/–	Hi-z/–	I	t8
M17	EINT4/GPF4	GPF4	–/–	Hi-z/–	I	t8
L14	EINT5/GPF5	GPF5	–/–	Hi-z/–	I	t8
L15	EINT6/GPF6	GPF6	–/–	Hi-z/–	I	t8
L16	EINT7/GPF7	GPF7	–/–	Hi-z/–	I	t8
N9	EINT8/GPG0	GPG0	–/–	Hi-z/–	I	t8
T9	EINT9/GPG1	GPG1	–/–	Hi-z/–	I	t8
J10	EINT10/nSS0/GPG2	GPG2	–/–/–	Hi-z/Hi-z/–	I	t8
R10	EINT11/nSS1/GPG3	GPG3	–/–/–	Hi-z/Hi-z/–	I	t8
P11	EINT12/LCD_PWREN/GPG4	GPG4	–/–/–	Hi-z/O(L)/–	I	t8
K10	EINT13/SPIMISO1/GPG5	GPG5	–/–/–	Hi-z/Hi-z/–	I	t8
R11	EINT14/SPIMOSI1/GPG6	GPG6	–/–/–	Hi-z/Hi-z/–	I	t8
L10	EINT15/SPICLK1/GPG7	GPG7	–/–/–	Hi-z/Hi-z/–	I	t8

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表 1-2 。 s3c2440a 289 引脚 fbga 的管脚分配（表 4/9） （续） ）

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
T10	EINT16/GPG8	GPG8	–/–	Hi-z/–	I	t8
M11	EINT17/nRTS1/GPG9	GPG9	–/–/–	Hi-z/O(H)/–	I	t8
N10	EINT18/nCTS1/GPG10	GPG10	–/–/–	Hi-z/Hi-z/–	I	t8
U12	EINT19/TCLK1/GPG11	GPG11	–/–/–	Hi-z/Hi-z/–	I	t12
M10	EINT20/GPG12	GPG12	–/–	Hi-z/–	I	t12
T11	EINT21/GPG13	GPG13	–/–	Hi-z/–	I	t12
L11	EINT22/GPG14	GPG14	–/–	Hi-z/–	I	t12
U13	EINT23/GPG15	GPG15	–/–	Hi-z/–	I	t12
H12	EXTCLK	EXTCLK	–	–	AI	is
P17	UPLLCAP	UPLLCAP	–	–	AI	r50
N14	MPLLCAP	MPLLCAP	–	–	AI	r50
H14	nBATT_FLT	nBATT_FLT	–	–	I	is
D4	nBE0	nBE0	Hi-z	Hi-z,O(H)	O(H)	t10s
B5	nBE1	nBE1	Hi-z	Hi-z,O(H)	O(H)	t10s
D5	nBE2	nBE2	Hi-z	Hi-z,O(H)	O(H)	t10s
E5	nBE3	nBE3	Hi-z	Hi-z,O(H)	O(H)	t10s
R12	NCON	NCON	–	–	I	is
G6	FRnB	FRnB	–	Hi-z,O(L)	I	d2s
F3	nFWE/GPA19	GPA19	O(H)/–	Hi-z,O(H)/–	O(H)	t10s
E1	nFRE/GPA20	GPA20	O(H)/–	Hi-z,O(H)/–	O(H)	t10s
F4	nFCE/GPA22	GPA22	O(H)/–	Hi-z,O(H)/–	O(H)	t10s
F5	CLE/GPA17	GPA17	O(L)/–	Hi-z,O(L)/–	O(L)	t10s
D1	ALE/GPA18	GPA18	O(L)/–	Hi-z,O(L)/–	O(L)	t10s
N13	nRSTOUT/GPA21	GPA21	–/–	O(L)/–	O(L)	b8
C5	nOE	nOE	Hi-z	Hi-z,O(H)	O(H)	t10s
H16	nRESET	nRESET	–	–	I	is
F6	nGCS0	nGCS0	Hi-z	Hi-z,O(H)	O(H)	t10s
B2	nGCS1/GPA12	GPA12	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
C3	nGCS2/GPA13	GPA13	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
C4	nGCS3/GPA14	GPA14	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
D3	nGCS4/GPA15	GPA15	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
C2	nGCS5/GPA16	GPA16	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
D2	nGCS6	nGCS6	Hi-z	Hi-z,O(H)	O(H)	t10s

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表 1-2 。 s3c2440a 289 引脚 fbga 的管脚分配（表 5/9） （续） ）

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
E3	nGCS7	nGCS7	Hi-z	Hi-z,O(H)	O(H)	t10s
D6	nSCAS	nSCAS	Hi-z	Hi-z,O(H)	O(H)	t10s
C6	nSRAS	nSRAS	Hi-z	Hi-z,O(H)	O(H)	t10s
H15	nTRST	nTRST	I	–	I	is
E4	nWAIT	nWAIT	–	Hi-z,O(L)	I	d2s
E6	nWE	nWE	Hi-z	Hi-z,O(H)	O(H)	t10s
J6	TOUT0/GPB0	GPB0	–/–	O(L)/–	I	t8
J5	TOUT1/GPB1	GPB1	–/–	O(L)/–	I	t8
J7	TOUT2/GPB2	GPB2	–/–	O(L)/–	I	t8
K3	TOUT3/GPB3	GPB3	–/–	O(L)/–	I	t8
K4	TCLK0/GPB4	GPB4	–/–	–/–	I	t8
K2	nXBACK/GPB5	GPB5	–/–	O(H)/–	I	t8
L5	nXBREQ/GPB6	GPB6	–/–	–/–	I	t8
K7	nXDACK1/GPB7	GPB7	–/–	O(H)/–	I	t8
K5	nXDREQ1/GPB8	GPB8	–/–	–/–	I	t8
L3	nXDACK0/GPB9	GPB9	–/–	O(H)/–	I	t8
K6	nXDREQ0/GPB10	GPB10	–/–	–/–	I	t8
T15	OM0	OM0	–	–	I	is
R13	OM1	OM1	–	–	I	is
P13	OM2	OM2	–	–	I	is
T13	OM3	OM3	–	–	I	is
J12	PWREN	PWREN	O(H)	O(L)	O(H)	b8
K11	nCTS0/GPH0	GPH0	–/–	–/–	I	t8
L17	nRTS0/GPH1	GPH1	–/–	O(H)/–	I	t8
K13	TXD0/GPH2	GPH2	–/–	O(H)/–	I	t8
K14	RXD0/GPH3	GPH3	–/–	–/–	I	t8
K16	TXD1/GPH4	GPH4	–/–	O(H)/–	I	t8
K17	RXD1/GPH5	GPH5	–/–	–/–	I	t8
J11	TXD2/nRTS1/GPH6	GPH6	–/–/–	O(H)/O(H)/–	I	t8
J15	RXD2/nCTS1/GPH7	GPH7	–/–/–	Hi-z/Hi-z/–	I	t8
K15	UEXTCLK/GPH8	GPH8	–/–	Hi-z/–	I	t8
R9	CLKOUT0/GPH9	GPH9	–/–	O(L)/–	I	t12
P10	CLKOUT1/GPH10	GPH10	–/–	O(L)/–	I	t12

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表 1-2 。 s3c2440a 289 引脚 fbga 的管脚分配（表 6/9） （续） ）

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
A2	SCKE	SCKE	Hi-z	O(L)	O(H)	t10s
B4	SCLK0	SCLK0	Hi-z	O(L)	O(SCLK)	t12s
B3	SCLK1	SCLK1	Hi-z	O(L)	O(SCLK)	t12s
P7	I2SLRCK/AC_SYNC	GPE0	–/–	Hi-z/–	I	t8
R7	I2SSCLK/AC_BIT_CLK	GPE1	–/–	Hi-z/–	I	t8
T7	CDCLK/AC_nRESET	GPE2	–/–	Hi-z/–	I	t8
L8	I2SSDI/AC_SDATA_IN	GPE3	–/–/–	Hi-z/Hi-z/–	I	t8
U6	I2SSDO/AC_SDATA_OUT	GPE4	–/–/–	O(L)/Hi-z/–	I	t8
N8	SDCLK/GPE5	GPE5	–/–	O(L)/–	I	t8
K8	SDCMD/GPE6	GPE6	–/–	Hi-z/–	I	t8
R8	SDDAT0/GPE7	GPE7	–/–	Hi-z/–	I	t8
M8	SDDAT1/GPE8	GPE8	–/–	Hi-z/–	I	t8
P8	SDDAT2/GPE9	GPE9	–/–	Hi-z/–	I	t8
J9	SDDAT3/GPE10	GPE10	–/–	Hi-z/–	I	t8
K9	SPIMISO0/GPE11	GPE11	–/–	Hi-z/–	I	t8
P9	SPIMOSI0/GPE12	GPE12	–/–	Hi-z/–	I	t8
L9	SPICLK0/GPE13	GPE13	–/–	Hi-z/–	I	t8
U8	IICSCL/GPE14	GPE14	–/–	Hi-z/–	I	d8
M9	IICSDA/GPE15	GPE15	–/–	Hi-z/–	I	d8
J13	TCK	TCK	I	–	I	is
H17	TDI	TDI	I	–	I	is
J16	TDO	TDO	O	O	O	ot
J14	TMS	TMS	I	–	I	is
L1	LEND/GPC0	GPC0	–/–	O(L)/–	I	t8
L4	VCLK/GPC1	GPC1	–/–	O(L)/–	I	t8
M1	VLINE/GPC2	GPC2	–/–	O(L)/–	I	t8
L7	VFRAME/GPC3	GPC3	–/–	O(L)/–	I	t8
M4	VM/GPC4	GPC4	–/–	O(L)/–	I	t8
M3	LCD_LPCOE/GPC5	GPC5	–/–	O(L)/–	I	t8
M2	LCD_LPCREV/GPC6	GPC6	–/–	O(L)/–	I	t8
P1	LCD_LPCREVB/GPC7	GPC7	–/–	O(L)/–	I	t8
N2	VD0/GPC8	GPC8	–/–	O(L)/–	I	t8
L6	VD1/GPC9	GPC9	–/–	O(L)/–	I	t8

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表 1-2 。 s3c2440a 289 引脚 fbga 的管脚分配（表 7/9） （续） ）

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
N4	VD2/GPC10	GPC10	–/–	O(L)/–	I	t8
R1	VD3/GPC11	GPC11	–/–	O(L)/–	I	t8
N3	VD4/GPC12	GPC12	–/–	O(L)/–	I	t8
P2	VD5/GPC13	GPC13	–/–	O(L)/–	I	t8
M6	VD6/GPC14	GPC14	–/–	O(L)/–	I	t8
P3	VD7/GPC15	GPC15	–/–	O(L)/–	I	t8
R2	VD8/GPD0	GPD0	–/–	O(L)/–	I	t8
M5	VD9/GPD1	GPD1	–/–	O(L)/–	I	t8
N5	VD10/GPD2	GPD2	–/–	O(L)/–	I	t8
R3	VD11/GPD3	GPD3	–/–	O(L)/–	I	t8
P4	VD12/GPD4	GPD4	–/–	O(L)/–	I	t8
R4	VD13/ GPD5	GPD5	–/–/–	O(L)/O/–	I	t8
P5	VD14/GPD6	GPD6	–/–/–	O(L)/O/–	I	t8
N6	VD15/GPD7	GPD7	–/–/–	O(L)/O/–	I	t8
M7	VD16/SPIMISO1/GPD8	GPD8	–/–/–	O(L)/Hi-z/–	I	t8
T4	VD17/SPIMOSI1/GPD9	GPD9	–/–/–	O(L)/Hi-z/–	I	t8
R5	VD18/SPICLK1/GPD10	GPD10	–/–/–	O(L)/Hi-z/–	I	t8
T5	VD19//GPD11	GPD11	–/–/–	O(L)/Hi-z/–	I	t8
P6	VD20/ GPD12	GPD12	–/–/–	O(L)/Hi-z/–	I	t8
R6	VD21/ GPD13	GPD13	–/–/–	O(L)/Hi-z/–	I	t8
N7	VD22/nSS1/GPD14	GPD14	–/–/–	O(L)/Hi-z/–	I	t8
U5	VD23/nSS0/GPD15	GPD15	–/–/–	O(L)/Hi-z/–	I	t8
U16	Vref	Vref	–	–	AI	ia
G14	XTIpll	XTIpll	–	–	AI	m26
M14	Xtirtc	Xtirtc	–	–	AI	nc
G15	XTOpll	XTOpll	–	–	AO	m26
L12	Xtortc	Xtortc	–	–	AO	nc
N15	VDD_RTC	VDD_RTC	P	P	P	drtc
P14	VDDA_ADC	VDDA_ADC	P	P	P	d33th
N16	VDDA_MPLL	VDDA_MPLL	P	P	P	d12t
M13	VDDA_UPLL	VDDA_UPLL	P	P	P	d12t
G4	VDDalive	VDDalive	P	P	P	d12i
J17	VDDalive	VDDalive	P	P	P	d12i

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表 1-2 。 s3c2440a 289 引脚 fbga 的管脚分配（表 8/9） （续） ）

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
A1	VDDi	VDDi	P	P	P	d12c
A10	VDDi	VDDi	P	P	P	d12c
A16	VDDi	VDDi	P	P	P	d12c
A6	VDDi	VDDi	P	P	P	d12c
B11	VDDi	VDDi	P	P	P	d12c
F1	VDDi	VDDi	P	P	P	d12c
F16	VDDi	VDDi	P	P	P	d12c
U11	VDDi	VDDi	P	P	P	d12c
L2	VDDiarm	VDDiarm	P	P	P	d12c
T6	VDDiarm	VDDiarm	P	P	P	d12c
T8	VDDiarm	VDDiarm	P	P	P	d12c
U1	VDDiarm	VDDiarm	P	P	P	d12c
J2	VDDiarm	VDDiarm	P	P	P	d12c
U2	VDDiarm	VDDiarm	P	P	P	d12c
A9	VDDMOP	VDDMOP	P	P	P	d33o
B12	VDDMOP	VDDMOP	P	P	P	d33o
B14	VDDMOP	VDDMOP	P	P	P	d33o
B16	VDDMOP	VDDMOP	P	P	P	d33o
B6	VDDMOP	VDDMOP	P	P	P	d33o
C1	VDDMOP	VDDMOP	P	P	P	d33o
F17	VDDMOP	VDDMOP	P	P	P	d33o
J1	VDDOP	VDDOP	P	P	P	d33o
T12	VDDOP	VDDOP	P	P	P	d33o
T3	VDDOP	VDDOP	P	P	P	d33o
K12	VDDOP	VDDOP	P	P	P	d33o
T14	VSSA_ADC	VSSA_ADC	P	P	P	sth
R17	VSSA_MPLL	VSSA_MPLL	P	P	P	st
M12	VSSA_UPLL	VSSA_UPLL	P	P	P	st
A12	VSSi	VSSi	P	P	P	si
A3	VSSi	VSSi	P	P	P	si
A4	VSSi	VSSi	P	P	P	si
B10	VSSi	VSSi	P	P	P	si
C17	VSSi	VSSi	P	P	P	si

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表 1-2 。 s3c2440a 289 引脚 fbga 的管脚分配（表 9/9） （续） ）

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
F2	VSSi	VSSi	P	P	P	si
G17	VSSi	VSSi	P	P	P	si
H1	VSSiarm	VSSiarm	P	P	P	si
K1	VSSiarm	VSSiarm	P	P	P	si
T1	VSSiarm	VSSiarm	P	P	P	si
T2	VSSiarm	VSSiarm	P	P	P	si
U10	VSSiarm	VSSiarm	P	P	P	si
U4	VSSiarm	VSSiarm	P	P	P	si
U7	VSSiarm	VSSiarm	P	P	P	si
A11	VSSMOP	VSSMOP	P	P	P	so
A15	VSSMOP	VSSMOP	P	P	P	so
A5	VSSMOP	VSSMOP	P	P	P	so
A7	VSSMOP	VSSMOP	P	P	P	so
B1	VSSMOP	VSSMOP	P	P	P	so
B13	VSSMOP	VSSMOP	P	P	P	so
D16	VSSMOP	VSSMOP	P	P	P	so
D17	VSSMOP	VSSMOP	P	P	P	so
E2	VSSMOP	VSSMOP	P	P	P	so
G1	VSSOP	VSSOP	P	P	P	so
N1	VSSOP	VSSOP	P	P	P	so
U15	VSSOP	VSSOP	P	P	P	so
U3	VSSOP	VSSOP	P	P	P	so
U9	VSSOP	VSSOP	P	P	P	so
H11	VSSOP	VSSOP	P	P	P	so

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注释：

1 。@BUS REQ 表示处于外部总线控制状态，即总线被其他总线所有者占用。

2 。“-”标记表示在BUS REQ 模式中引脚没有变化。

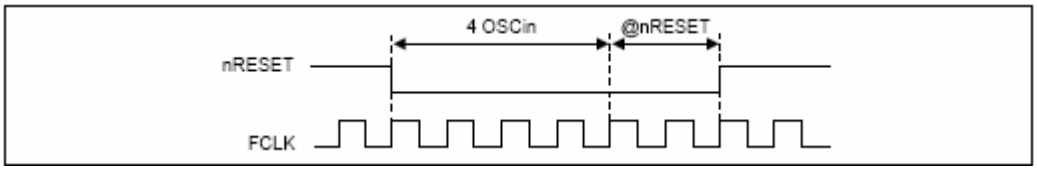
3 。Hi-z 或Pre 表示高阻状态或保持之前的状态，究竟是哪一个由MISCCR 寄存器的设置决

定。

4 。AI/AO表示模拟输入/模拟输出。

5 。P, I, 和 O分别表示电源，输入和输出。

6。I/O 状态@nRESET 表示 I/O 脚在复位脚 nRESET 处于低电平下的状态，如下图所示。



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下表说明我 I/O 类型和描述。

Input (I)/Output (O) Type	Descriptions
d12i(vdd12ih)	1.2V V_{DD} for alive power
d12c(vdd12ih_core), si(vssih)	1.2V V_{DD}/V_{SS} for internal logic
d33o(vdd33oph), so(vssoph)	3.3V V_{DD}/V_{SS} for external logic
d33th(vdd33th_abb),sth(vssbbh_abb)	3.3V V_{DD}/V_{SS} for analog circuitry
d12t(vdd12t_abb), st(vssbb_abb)	1.2V V_{DD}/V_{SS} for analog circuitry
drtc(vdd30th_rtc)	3.0V V_{DD} for RTC power
t8(phbsu100ct8sm)	Bi-directional pad, LVCMOS schmitt-trigger, 100kΩ pull-up resistor with control, tri-state, Io = 8mA
is(phis)	Input pad, LVCMOS schmitt-trigger level
us(pbusb0)	USB pad
t10(phtot10cd)	5V tolerant output pad, tri-state.
ot(phot8)	Output pad, tri-state, Io = 8mA
b8(phob8)	Output pad, Io = 8mA
t16(phot16sm)	Output pad, tri-state, medium slew rate, Io = 16mA
r10(phiar10_abb)	Analog input pad with 10Ω resistor
ia(phia_abb)	Analog input pad
gp(phgpad_option)	Pad for analog pin
m26(phsoscm26_2440a)	Oscillator cell with enable and feedback resistor
t12(phbsu100ct12sm)	Bi-directional pad, LVCMOS schmitt-trigger, 100kΩ pull-up resistor with control, tri-state, Io = 12mA
d8(phbsd8sm)	Bi-directional pad, LVCMOS schmitt-trigger, open drain, Io = 8mA
t10s(phtot10cd_10_2440a)	output pad, LVCMOS, tri -state, output drive strenth control, Io = 4, 6, 8, 10mA
b12s(phtbsu100ct12cd_12_2440a)	Bi-directional pad, LVCMOS schmitt-trigger, 100kΩ pull-up resistor with control, tri -state, output drive strenth control, Io = 6, 8, 10, 12mA
d2s(phtbsd2_2440a)	Bi-directional pad, LVCMOS schmitt-trigger, open-drain, output drive strenth control,
r50(phoar50_abb)	Analog output pad, 50kΩ resistor, separated bulk-bias
t12s(phtot12cd_12_2440a)	output pad, LVCMOS, tri -state, output drive strenth control, Io = 6, 8, 10, 12mA
nc(phnc)	No connection pad

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信号说明

表 1-3 。 s3c2440a 信号说明（表 1/6 ）

Signal	Input/Output	Descriptions	
Bus Controller			
OM[1:0]	I	OM[1:0] sets S3C2440A in the TEST mode, which is used only at fabrication. Also, it determines the bus width of nGCS0. The pull-up/down resistor determines the logic level during RESET cycle. 00: Nand-boot 01: 16-bit 10: 32-bit 11: Test mode	
ADDR[26:0]	O	ADDR[26:0] (Address Bus) outputs the memory address of the corresponding bank .	
DATA[31:0]	IO	DATA[31:0] (Data Bus) inputs data during memory read and outputs data during memory write. The bus width is programmable among 8/16/32-bit.	
nGCS[7:0]	O	nGCS[7:0] (General Chip Select) are activated when the address of a memory is within the address region of each bank. The number of access cycles and the bank size can be programmed.	
nWE	O	nWE (Write Enable) indicates that the current bus cycle is a write cycle.	
nOE	O	nOE (Output Enable) indicates that the current bus cycle is a read cycle.	
nXBREQ	I	nXBREQ (Bus Hold Request) allows another bus master to request control of the local bus. BACK active indicates that bus control has been granted.	
nXBACK	O	nXBACK (Bus Hold Acknowledge) indicates that the S3C2440A has surrendered control of the local bus to another bus master.	
nWAIT	I	nWAIT requests to prolong a current bus cycle. As long as nWAIT is L, the current bus cycle cannot be completed.	
SDRAM/SRAM			
nSRAS	O	SDRAM row address strobe	
nSCAS	O	SDRAM column address strobe	
nSCS[1:0]	O	SDRAM chip select	
DQM[3:0]	O	SDRAM data mask	
SCLK[1:0]	O	SDRAM clock	
SCKE	O	SDRAM clock enable	
nBE[3:0]	O	Upper byte/lower byte enable (In case of 16-bit SRAM)	
nWBE[3:0]	O	Write byte enable	
NAND Flash			
CLE	O	Command latch enable	
ALE	O	Address latch enable	
nFCE	O	Nand flash chip enable	
nFRE	O	Nand flash read enable	
nFWE	O	Nand flash write enable	
NCON	I	Nand flash configuration	* If NAND flash controller isn't used, it has to be pull-up. (VDDMOP)
FRnB	I	Nand flash ready/busy	

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表 1-3 。 s3c2440a 信号说明（表 2/6 ）

Signal	Input/ Output	Descriptions
LCD Control Unit		
VD[23:0]	O	**STN/TFT/SEC TFT:** LCD data bus
LCD_PWREN	O	**STN/TFT/SEC TFT:** LCD panel power enable control signal
VCLK	O	**STN/TFT:** LCD clock signal
VFRAME	O	**STN:** LCD frame signal
VLINE	O	**STN:** LCD line signal
VM	O	**STN:** VM alternates the polarity of the row and column voltage
VSYNC	O	**TFT:** Vertical synchronous signal
HSYNC	O	**TFT:** Horizontal synchronous signal
VDEN	O	**TFT:** Data enable signal
LEND	O	**TFT:** Line end signal
STV	O	**SEC TFT:** SEC(Samsung Electronics Company) TFT LCD panel control signal
CPV	O	**SEC TFT:** SEC(Samsung Electronics Company) TFT LCD panel control signal
LCD_HCLK	O	**SEC TFT:** SEC(Samsung Electronics Company) TFT LCD panel control signal
TP	O	**SEC TFT:** SEC(Samsung Electronics Company) TFT LCD panel control signal
STH	O	**SEC TFT:** SEC(Samsung Electronics Company) TFT LCD panel control signal
LCD_LPCOE	O	**SEC TFT:** Timing control signal for specific TFT LCD
LCD_LPCREV	O	**SEC TFT:** Timing control signal for specific TFT LCD
LCD_LPCREVB	O	**SEC TFT:** Timing control signal for specific TFT LCD
CAMERA Interface		
CAMRESET	O	Software reset to the camera
CAMCLKOUT	O	Master clock to the camera
CAMPCLK	I	Pixel clock from camera
CAMHREF	I	Horizontal sync signal from camera
CAMVSYNC	I	Vertical sync signal from camera
CAMDATA[7:0]	I	Pixel data of YCbCr
Interrupt Control Unit		
EINT[23:0]	I	External interrupt request
DMA		
nXDREQ[1:0]	I	External DMA request
nXDACK[1:0]	O	External DMA acknowledge

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表 1-3 。 s3c2440a 信号说明（表 3/6 ）

Signal	Input/Output	Descriptions
UART		
RxD[2:0]	I	UART receives data input
TxD[2:0]	O	UART transmits data output
nCTS[1:0]	I	UART clear to send input signal
nRTS[1:0]	O	UART request to send output signal
UEXTCLK	I	External clock input for UART
ADC		
AIN[7:0]	AI	ADC input[7:0]. If it isn't used pin, it has to be low (ground).
Vref	AI	ADC Vref
IIC-Bus		
IICSDA	IO	IIC-bus data
IICSCL	IO	IIC-bus clock
IIS-Bus		
I2SLRCK	IO	IIS-bus channel select clock
I2SSDO	O	IIS-bus serial data output
I2SSDI	I	IIS-bus serial data input
I2SSCLK	IO	IIS-bus serial clock
CDCLK	O	CODEC system clock
AC'97		
AC_SYNC		48kHz fixed rate sample sync
AC_BIT_CLK	IO	12.288MHz serial data clock
AC_nRESET	O	AC'97 Master H/W Reset
AC_SDATA_IN	I	Serial, time division multiplexed, AC'97 input stream
AC_SDATA_OUT	O	Serial, time division multiplexed, AC'97 output stream
Touch Screen		
nXPON	O	Plus X-axis on-off control signal
XMON	O	Minus X-axis on-off control signal
nYPON	O	Plus Y-axis on-off control signal
YMON	O	Minus Y-axis on-off control signal
USB Host		
DN[1:0]	IO	DATA(–) from USB host. (Need to 15kΩ pull-down)
DP[1:0]	IO	DATA(+) from USB host. (Need to 15kΩ pull-down)
USB Device		
PDN0	IO	DATA(–) for USB peripheral. (Need to 470kΩ pull-down for power consumption in sleep mode)
PDP0	IO	DATA(+) for USB peripheral. (Need to 1.5kΩ pull-up)

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表 1-3 。 s3c2440a 信号说明（表 4/6 ）

Signal	Input/Output	Description
SPI		
SPIMISO[1:0]	IO	SPIMISO is the master data input line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role.
SPIMOSI[1:0]	IO	SPIMOSI is the master data output line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role.
SPICLK[1:0]	IO	SPI clock
nSS[1:0]	I	SPI chip select(only for slave mode)
SD		
SDDAT[3:0]	IO	SD receive/transmit data
SDCMD	IO	SD receive response/ transmit command
SDCLK	O	SD clock
General Port		
GPn[129:0]	IO	General input/output ports (some ports are output only)
TIMMER/PWM		
TOUT[3:0]	O	Timer output[3:0]
TCLK[1:0]	I	External timer clock input
JTAG TEST LOGIC		
nTRST	I	nTRST (TAP Controller Reset) resets the TAP controller at start. If debugger is used, A 10K pull-up resistor has to be connected. If debugger (black ICE) is not used, nTRST pin must be issued by a low active pulse (Typically connected to nRESET).
TMS	I	TMS (TAP Controller Mode Select) controls the sequence of the TAP controller's states. A 10K pull-up resistor has to be connected to TMS pin.
TCK	I	TCK (TAP Controller Clock) provides the clock input for the JTAG logic. A 10K pull-up resistor must be connected to TCK pin.
TDI	I	TDI (TAP Controller Data Input) is the serial input for test instructions and data. A 10K pull-up resistor must be connected to TDI pin.
TDO	O	TDO (TAP Controller Data Output) is the serial output for test instructions and data.

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表 1-3 。 s3c2440a 信号说明（表 5/6 ）

Signal	Input/Output	Description
Reset, Clock & Power		
XTOpll	AO	Crystal Output for internal osc circuit. When OM[3:2] = 00b, XTIpll is used for MPLL CLK source and UPLL CLK source. When OM[3:2] = 01b, XTIpll is used for MPLL CLK source only. When OM[3:2] = 10b, XTIpll is used for UPLL CLK source only. If it isn't used, it has to be a floating pin.
MPLLCAP	AI	Loop filter capacitor for main clock.
UPLLCAP	AI	Loop filter capacitor for USB clock.
XTIrtc	AI	32 kHz crystal input for RTC. If it isn't used, it has to be High (VDDRTC).
XTOrtc	AO	32 kHz crystal output for RTC. If it isn't used, it has to be Float.
CLKOUT[1:0]	O	Clock output signal. The CLKSEL of MISCCR register configures the clock output mode among the MPLL CLK, UPLL CLK, FCLK, HCLK, PCLK.
nRESET	ST	nRESET suspends any operation in progress and places S3C2440A into a known reset state. For a reset, nRESET must be held to L level for at least 4 OSCin after the processor power has been stabilized.
nRSTOUT	O	For external device reset control (nRSTOUT = nRESET & nWDTRST & SW_RESET)
PWREN	O	1.2V/1.3V core power on-off control signal
nBATT_FLT	I	Probe for battery state(Does not wake up at Sleep mode in case of low battery state). If it isn't used, it has to be High (VDDOP).
OM[3:2]	I	OM[3:2] determines how the clock is made. OM[3:2] = 00b, Crystal is used for MPLL CLK source and UPLL CLK source. OM[3:2] = 01b, Crystal is used for MPLL CLK source and EXTCLK is used for UPLL CLK source. OM[3:2] = 10b, EXTCLK is used for MPLL CLK source and Crystal is used for UPLL CLK source. OM[3:2] = 11b, EXTCLK is used for MPLL CLK source and UPLL CLK source.
EXTCLK	I	External clock source. When OM[3:2] = 11b, EXTCLK is used for MPLL CLK source and UPLL CLK source. When OM[3:2] = 10b, EXTCLK is used for MPLL CLK source only. When OM[3:2] = 01b, EXTCLK is used for UPLL CLK source only. If it isn't used, it has to be High (VDDOP).
XTIpll	AI	Crystal Input for internal osc circuit. When OM[3:2] = 00b, XTIpll is used for MPLL CLK source and UPLL CLK source. When OM[3:2] = 01b, XTIpll is used for MPLL CLK source only. When OM[3:2] = 10b, XTIpll is used for UPLL CLK source only. If it isn't used, XTIpll has to be High (VDDOP).

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表 1-3 。 s3c2440a 信号说明（表 6/6 ）

Signal	Input/Output	Description
Power		
VDDalive	P	S3C2440A reset block and port status register V_{DD}. It should be always supplied whether in normal mode or in Sleep mode.
VDDiarm	P	S3C2440A core logic V_{DD} for ARM core.
VDDi	P	S3C2440A core logic V_{DD} for Internal block.
VSSi/VSSiarm	P	S3C2440A core logic V_{SS}
VDDi_MPLL	P	S3C2440A MPLL analog and digital V_{DD}.
VSSi_MPLL	P	S3C2440A MPLL analog and digital V_{SS}.
VDDOP	P	S3C2440A I/O port VDD (3.3V)
VDDMOP	P	S3C2440A memory I/O V_{DD} 3.3V: SCLK up to 135 MHz 2.5V: SCLK up to 135 MHz 1.8V: SCLK up to 93 MHz
VSSOP	P	S3C2440A I/O port VSS
RTCVDD	P	RTC V_{DD} (3.0V, Input range: 1.8 ~ 3.3V) This pin must be connected to power properly if RTC isn't used.
VDDi_UPLL	P	S3C2440A UPLL analog and digital V_{DD}
VSSi_UPLL	P	S3C2440A UPLL analog and digital V_{SS}
VDDA_ADC	P	S3C2440A ADC V_{DD}(3.3V)
VSSA_ADC	P	S3C2440A ADC V_{SS}

注释：

1 。I/O：输入/输出。

2 。AI/AO：表示模拟输入/模拟输出

3 。ST ： 施密特触发。

4 。P：表示电源。

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s3c2440a特殊寄存器

表 1-4 。 s3c2440a 特殊寄存器（表 1/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
Memory Controllers					
BWSCON	0x48000000		W	R/W	Bus width & wait status control
BANKCON0	0x48000004				Boot ROM control
BANKCON1	0x48000008				BANK1 control
BANKCON2	0x4800000C				BANK2 control
BANKCON3	0x48000010				BANK3 control
BANKCON4	0x48000014				BANK4 control
BANKCON5	0x48000018				BANK5 control
BANKCON6	0x4800001C				BANK6 control
BANKCON7	0x48000020				BANK7 control
REFRESH	0x48000024				DRAM/SDRAM refresh control
BANKSIZE	0x48000028				Flexible bank size
MRSRB6	0x4800002C				Mode register set for SDRAM BANK6
MRSRB7	0x48000030				Mode register set for SDRAM BANK7

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表 1-4 。 s3c2440a 特殊寄存器（表 2/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
USB Host Controller					
HcRevision	0x49000000	←	W		Control and status group
HcControl	0x49000004				
HcCommonStatus	0x49000008				
HcInterruptStatus	0x4900000C				
HcInterruptEnable	0x49000010				
HcInterruptDisable	0x49000014				
HcHCCA	0x49000018				Memory pointer group
HcPeriodCuttentED	0x4900001C				
HcControlHeadED	0x49000020				
HcControlCurrentED	0x49000024				
HcBulkHeadED	0x49000028				
HcBulkCurrentED	0x4900002C				
HcDoneHead	0x49000030				Frame counter group
HcRmInterval	0x49000034				
HcFmRemaining	0x49000038				
HcFmNumber	0x4900003C				
HcPeriodicStart	0x49000040				
HcLSThreshold	0x49000044				
HcRhDescriptorA	0x49000048				Root hub group
HcRhDescriptorB	0x4900004C				
HcRhStatus	0x49000050				
HcRhPortStatus1	0x49000054				
HcRhPortStatus2	0x49000058				
Interrupt Controller					
SRCPND	0X4A000000	←	W	R/W	Interrupt request status
INTMOD	0X4A000004			W	Interrupt mode control
INTMSK	0X4A000008			R/W	Interrupt mask control
PRIORITY	0X4A00000C			W	IRQ priority control
INTPND	0X4A000010			R/W	Interrupt request status
INTOFFSET	0X4A000014			R	Interrupt request source offset
SUBSRCPND	0X4A000018			R/W	Sub source pending
INTSUBMSK	0X4A00001C			R/W	Interrupt sub mask

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表 1-4 。 s3c2440a 特殊寄存器（表 3/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
DMA					
DISRC0	0x4B000000	←	W	R/W	DMA 0 initial source
DISRCC0	0x4B000004				DMA 0 initial source control
DIDST0	0x4B000008				DMA 0 initial destination
DIDSTC0	0x4B00000C				DMA 0 initial destination control
DCON0	0x4B000010				DMA 0 control
DSTAT0	0x4B000014			R	DMA 0 count
DCSRC0	0x4B000018				DMA 0 current source
DCDST0	0x4B00001C				DMA 0 current destination
DMASKTRIG0	0x4B000020			R/W	DMA 0 mask trigger
DISRC1	0x4B000040				DMA 1 initial source
DISRCC1	0x4B000044				DMA 1 initial source control
DIDST1	0x4B000048				DMA 1 initial destination
DIDSTC1	0x4B00004C				DMA 1 initial destination control
DCON1	0x4B000050				DMA 1 control
DSTAT1	0x4B000054			R	DMA 1 count
DCSRC1	0x4B000058				DMA 1 current source
DCDST1	0x4B00005C				DMA 1 current destination
DMASKTRIG1	0x4B000060			R/W	DMA 1 mask trigger
DISRC2	0x4B000080				DMA 2 initial source
DISRCC2	0x4B000084				DMA 2 initial source control
DIDST2	0x4B000088				DMA 2 initial destination
DIDSTC2	0x4B00008C				DMA 2 initial destination control
DCON2	0x4B000090				DMA 2 control
DSTAT2	0x4B000094			R	DMA 2 count
DCSRC2	0x4B000098				DMA 2 current source
DCDST2	0x4B00009C				DMA 2 current destination
DMASKTRIG2	0x4B0000A0			R/W	DMA 2 mask trigger
DISRC3	0x4B0000C0	←	W	R/W	DMA 3 initial source
DISRCC3	0x4B0000C4				DMA 3 initial source control
DIDST3	0x4B0000C8				DMA 3 initial destination
DIDSTC3	0x4B0000CC				DMA 3 initial destination control
DCON3	0x4B0000D0				DMA 3 control
DSTAT3	0x4B0000D4			R	DMA 3 count
DCSRC3	0x4B0000D8				DMA 3 current source
DCDST3	0x4B0000DC				DMA 3 current destination
DMASKTRIG3	0x4B0000E0			R/W	DMA 3 mask trigger

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表 1-4 。 s3c2440a 特殊寄存器（表 4/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
Clock & Power Management					
LOCKTIME	0x4C000000	←	W	R/W	PLL lock time counter
MPLLCON	0x4C000004				MPLL control
UPLLCON	0x4C000008				UPLL control
CLKCON	0x4C00000C				Clock generator control
CLKSLOW	0x4C000010				Slow clock control
CLKDIVN	0x4C000014				Clock divider control
CAMDIVN	0x4C000018				Camera clock divider control
LCD Controller					
LCDCON1	0X4D000000	←	W	R/W	LCD control 1
LCDCON2	0X4D000004				LCD control 2
LCDCON3	0X4D000008				LCD control 3
LCDCON4	0X4D00000C				LCD control 4
LCDCON5	0X4D000010				LCD control 5
LCDSADDR1	0X4D000014				STN/TFT: frame buffer start address 1
LCDSADDR2	0X4D000018				STN/TFT: frame buffer start address 2
LCDSADDR3	0X4D00001C				STN/TFT: virtual screen address set
REDLUT	0X4D000020				STN: red lookup table
GREENLUT	0X4D000024				STN: green lookup table
BLUELUT	0X4D000028				STN: blue lookup table
DITHMODE	0X4D00004C				STN: dithering mode
TPAL	0X4D000050				TFT: temporary palette
LCDINTPND	0X4D000054				LCD interrupt pending
LCDSRCPND	0X4D000058				LCD interrupt source
LCDINTMSK	0X4D00005C				LCD interrupt mask
TCONSEL	0X4D000060				TCON(LPC3600/LCC3600) control

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表 1-4 。 s3c2440a 特殊寄存器（表 5/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
NAND Flash					
NFCONF	0x4E000000	←	W	R/W	NAND flash configuration
NFCONT	0x4E000004				NAND flash control
NFCMD	0x4E000008				NAND flash command
NFADDR	0x4E00000C				NAND flash address
NFDATA	0x4E000010				NAND flash data
NFMECC0	0x4E000014				NAND flash main area ECC0/1
NFMECC1	0x4E000018				NAND flash main area ECC2/3
NFSECC	0x4E00001C				NAND flash spare area ECC
NFSTAT	0x4E000020				NAND flash operation status
NFESTAT0	0x4E000024				NAND flash ECC status for I/O[7:0]
NFESTAT1	0x4E000028				NAND flash ECC status for I/O[15:8]
NFMECC0	0x4E00002C			R	NAND flash main area ECC0 status
NFMECC1	0x4E000030				NAND flash main area ECC1 status
NFSECC	0x4E000034				NAND flash spare area ECC status
NFSBLK	0x4E000038			R/W	NAND flash start block address
NFEBLK	0x4E00003C				NAND flash end block address

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表 1-4 。 s3c2440a 特殊寄存器（表 6/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
Camera Interface					
CISRCFMT	0x4F000000	←	W	RW	Input source format
CIWDOFST	0x4F000004				Window offset register
CIGCTRL	0x4F000008				Global control register
CICOYSA1	0x4F000018				Y 1st frame start address for codec DMA
CICOYSA2	0x4F00001C				Y 2nd frame start address for codec DMA
CICOYSA3	0x4F000020				Y 3nd frame start address for codec DMA
CICOYSA4	0x4F000024				Y 4th frame start address for codec DMA
CICOCBSA1	0x4F000028				Cb 1st frame start address for codec DMA
CICOCBSA2	0x4F00002C				Cb 2nd frame start address for codec DMA
CICOCBSA3	0x4F000030				Cb 3nd frame start address for codec DMA
CICOCBSA4	0x4F000034				Cb 4th frame start address for codec DMA
CICOCRSA1	0x4F000038				Cr 1st frame start address for codec DMA
CICOCRSA2	0x4F00003C				Cr 2nd frame start address for codec DMA
CICOCRSA3	0x4F000040				Cr 3nd frame start address for codec DMA
CICOCRSA4	0x4F000044				Cr 4th frame start address for codec DMA
CICOTRGFMT	0x4F000048				Target image format of codec DMA
CICOCTRL	0x4F00004C				Codec DMA control related
CICOSCPRERATIO	0x4F000050				Codec pre-scaler ratio control
CICOSCPREDST	0x4F000054				Codec pre-scaler destination format
CICOSCCTRL	0x4F000058				Codec main-scaler control
CICOTAREA	0x4F00005C				Codec scaler target area
CICOSTATUS	0x4F000064				Codec path status
CIPRCLRSA1	0x4F00006C				RGB 1st frame start address for preview DMA
CIPRCLRSA2	0x4F000070				RGB 2nd frame start address for preview DMA
CIPRCLRSA3	0x4F000074				RGB 3nd frame start address for preview DMA
CIPRCLRSA4	0x4F000078				RGB 4th frame start address for preview DMA
CIPRTRGFMT	0x4F00007C				Target image format of preview DMA
CIPRCTRL	0x4F000080				Preview DMA control related
CIPRSCPRERATIO	0x4F000084				Preview pre-scaler ratio control
CIPRSCPREDST	0x4F000088				Preview pre-scaler destination format
CIPRSCCTRL	0x4F00008C				Preview main-scaler control
CIPRTAREA	0x4F000090				Preview scaler target area
CIPRSTATUS	0x4F000098				Preview path status
CIIMGCPT	0x4F0000A0				Image capture enable command

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表 1-4 。 s3c2440a 特殊寄存器（表 7/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
UART					
ULCON0	0x50000000	←	W	R/W	UART 0 line control
UCON0	0x50000004				UART 0 control
UFCON0	0x50000008				UART 0 FIFO control
UMCON0	0x5000000C				UART 0 modem control
UTRSTAT0	0x50000010			R	UART 0 Tx/Rx status
UERSTAT0	0x50000014				UART 0 Rx error status
UFSTAT0	0x50000018				UART 0 FIFO status
UMSTAT0	0x5000001C				UART 0 modem status
UTXH0	0x50000023	0x50000020	B	W	UART 0 transmission hold
URXH0	0x50000027	0x50000024		R	UART 0 receive buffer
UBRDIV0	0x50000028	←	W	R/W	UART 0 baud rate divisor
ULCON1	0x50004000				UART 1 line control
UCON1	0x50004004				UART 1 control
UFCON1	0x50004008				UART 1 FIFO control
UMCON1	0x5000400C				UART 1 modem control
UTRSTAT1	0x50004010			R	UART 1 Tx/Rx status
UERSTAT1	0x50004014				UART 1 Rx error status
UFSTAT1	0x50004018				UART 1 FIFO status
UMSTAT1	0x5000401C				UART 1 modem status
UTXH1	0x50004023	0x50004020	B	W	UART 1 transmission hold
URXH1	0x50004027	0x50004024		R	UART 1 receive buffer
UBRDIV1	0x50004028	←	W	R/W	UART 1 baud rate divisor
ULCON2	0x50008000				UART 2 line control
UCON2	0x50008004				UART 2 control
UFCON2	0x50008008				UART 2 FIFO control
UTRSTAT2	0x50008010			R	UART 2 Tx/Rx status
UERSTAT2	0x50008014				UART 2 Rx error status
UFSTAT2	0x50008018				UART 2 FIFO status
UTXH2	0x50008023	0x50008020	B	W	UART 2 transmission hold
URXH2	0x50008027	0x50008024		R	UART 2 receive buffer
UBRDIV2	0x50008028	←	W	R/W	UART 2 baud rate divisor

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表 1-4 。 s3c2440a 特殊寄存器（表 8/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
PWM Timer					
TCFG0	0x51000000	←	W	R/W	Timer configuration
TCFG1	0x51000004				Timer configuration
TCON	0x51000008				Timer control
TCNTB0	0x5100000C				Timer count buffer 0
TCMPB0	0x51000010				Timer compare buffer 0
TCNTO0	0x51000014			R	Timer count observation 0
TCNTB1	0x51000018			R/W	Timer count buffer 1
TCMPB1	0x5100001C				Timer compare buffer 1
TCNTO1	0x51000020			R	Timer count observation 1
TCNTB2	0x51000024			R/W	Timer count buffer 2
TCMPB2	0x51000028				Timer compare buffer 2
TCNTO2	0x5100002C			R	Timer count observation 2
TCNTB3	0x51000030			R/W	Timer count buffer 3
TCMPB3	0x51000034				Timer compare buffer 3
TCNTO3	0x51000038			R	Timer count observation 3
TCNTB4	0x5100003C			R/W	Timer count buffer 4
TCNTO4	0x51000040			R	Timer count observation 4

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表 1-4 。 s3c2440a 特殊寄存器（表 9/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
USB Device					
FUNC_ADDR_REG	0x52000143	0x52000140	B	R/W	Function address
PWR_REG	0x52000147	0x52000144			Power management
EP_INT_REG	0x5200014B	0x52000148			EP interrupt pending and clear
USB_INT_REG	0x5200015B	0x52000158			USB interrupt pending and clear
EP_INT_EN_REG	0x5200015F	0x5200015C			Interrupt enable
USB_INT_EN_REG	0x5200016F	0x5200016C			Interrupt enable
FRAME_NUM1_REG	0x52000173	0x52000170		R	Frame number lower byte
FRAME_NUM2_REG	0x52000177	0x52000174			Frame number higher byte
INDEX_REG	0x5200017B	0x52000178		R/W	Register index
EP0_CSR	0x52000187	0x52000184			Endpoint 0 status
IN_CSR1_REG	0x52000187	0x52000184			In endpoint control status
IN_CSR2_REG	0x5200018B	0x52000188			In endpoint control status
MAXP_REG	0x52000183	0x52000180			Endpoint max packet
OUT_CSR1_REG	0x52000193	0x52000190			Out endpoint control status
OUT_CSR2_REG	0x52000197	0x52000194			Out endpoint control status
OUT_FIFO_CNT1_REG	0x5200019B	0x52000198		R	Endpoint out write count
OUT_FIFO_CNT2_REG	0x5200019F	0x5200019C			Endpoint out write count
EP0_FIFO	0x520001C3	0x520001C0		R/W	Endpoint 0 FIFO
EP1_FIFO	0x520001C7	0x520001C4			Endpoint 1 FIFO
EP2_FIFO	0x520001CB	0x520001C8			Endpoint 2 FIFO
EP3_FIFO	0x520001CF	0x520001CC			Endpoint 3 FIFO
EP4_FIFO	0x520001D3	0x520001D0			Endpoint 4 FIFO
EP1_DMA_CON	0x52000203	0x52000200			EP1 DMA Interface control
EP1_DMA_UNIT	0x52000207	0x52000204			EP1 DMA Tx unit counter
EP1_DMA_FIFO	0x5200020B	0x52000208			EP1 DMA Tx FIFO counter
EP1_DMA_TTC_L	0x5200020F	0x5200020C			EP1 DMA Total Tx counter
EP1_DMA_TTC_M	0x52000213	0x52000210			EP1 DMA Total Tx counter
EP1_DMA_TTC_H	0x52000217	0x52000214			EP1 DMA Total Tx counter
EP2_DMA_CON	0x5200021B	0x52000218	B	R/W	EP2 DMA interface control
EP2_DMA_UNIT	0x5200021F	0x5200021C			EP2 DMA Tx Unit counter
EP2_DMA_FIFO	0x52000223	0x52000220			EP2 DMA Tx FIFO counter
EP2_DMA_TTC_L	0x52000227	0x52000224			EP2 DMA total Tx counter
EP2_DMA_TTC_M	0x5200022B	0x52000228			EP2 DMA total Tx counter

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表 1-4 。 s3c2440a 特殊寄存器（表 10/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
USB Device (Continued)					
EP2_DMA_TTC_H	0x5200022F	0x5200022C			EP2 DMA Total Tx counter
EP3_DMA_CON	0x52000243	0x52000240			EP3 DMA Interface control
EP3_DMA_UNIT	0x52000247	0x52000244			EP3 DMA Tx Unit counter
EP3_DMA_FIFO	0x5200024B	0x52000248			EP3 DMA Tx FIFO counter
EP3_DMA_TTC_L	0x5200024F	0x5200024C			EP3 DMA Total Tx counter
EP3_DMA_TTC_M	0x52000253	0x52000250			EP3 DMA Total Tx counter
EP3_DMA_TTC_H	0x52000257	0x52000254			EP3 DMA Total Tx counter
EP4_DMA_CON	0x5200025B	0x52000258			EP4 DMA Interface control
EP4_DMA_UNIT	0x5200025F	0x5200025C			EP4 DMA Tx Unit counter
EP4_DMA_FIFO	0x52000263	0x52000260			EP4 DMA Tx FIFO counter
EP4_DMA_TTC_L	0x52000267	0x52000264			EP4 DMA Total Tx counter
EP4_DMA_TTC_M	0x5200026B	0x52000268			EP4 DMA Total Tx counter
EP4_DMA_TTC_H	0x5200026F	0x5200026C			EP4 DMA Total Tx counter
Watchdog Timer					
WTCON	0x53000000	←	W	R/W	Watchdog timer mode
WTDAT	0x53000004				Watchdog timer data
WTCNT	0x53000008				Watchdog timer count
IIC					
IICCON	0x54000000	←	W	R/W	IIC control
IICSTAT	0x54000004				IIC status
IICADD	0x54000008				IIC address
IICDS	0x5400000C				IIC data shift
IICLC	0x54000010				IIC multi-master line control
IIS					
IISCON	0x55000000,02	0x55000000	HW,W	R/W	IIS control
IISMOD	0x55000004,06	0x55000004			IIS mode
IISPSR	0x55000008,0A	0x55000008			IIS prescaler
IISFCON	0x5500000C,0E	0x5500000C			IIS FIFO control
IISFIFO	0x55000012	0x55000010	HW		IIS FIFO entry

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表 1-4 。 s3c2440a 特殊寄存器（表 11/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
I/O port					
GPACON	0x56000000	←	W	R/W	Port A control
GPADAT	0x56000004				Port A data
GPBCON	0x56000010				Port B control
GPBDAT	0x56000014				Port B data
GPBUP	0x56000018				Pull-up control B
GPCCON	0x56000020				Port C control
GPCDAT	0x56000024				Port C data
GPCUP	0x56000028				Pull-up control C
GPDCON	0x56000030				Port D control
GPDDA1T	0x56000034				Port D data
GPDUP	0x56000038				Pull-up control D
GPECON	0x56000040				Port E control
GPEDAT	0x56000044				Port E data
GPEUP	0x56000048				Pull-up control E
GPFCON	0x56000050				Port F control
GPFDAT	0x56000054				Port F data
GPFUP	0x56000058				Pull-up control F
GPGCON	0x56000060				Port G control
GPGDAT	0x56000064				Port G data
GPGUP	0x56000068				Pull-up control G
GPHCON	0x56000070				Port H control
GPHDAT	0x56000074				Port H data
GPHUP	0x56000078				Pull-up control H
GPJCON	0x560000D0				Port J control
GPJDAT	0x560000D4				Port J data
GPJUP	0x560000D8				Pull-up control J
MISCCR	0x56000080				Miscellaneous control
DCLKCON	0x56000084				DCLK0/1 control
EXTINT0	0x56000088				External interrupt control register 0
EXTINT1	0x5600008C				External interrupt control register 1
EXTINT2	0x56000090				External interrupt control register 2

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表 1-4 。 s3c2440a 特殊寄存器（表 12/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
i/o port (continued)					
EINTFLT0	0x56000094	←	W	R/W	Reserved
EINTFLT1	0x56000098				Reserved
EINTFLT2	0x5600009C				External interrupt filter control register 2
EINTFLT3	0x560000A0				External interrupt filter control register 3
EINTMASK	0x560000A4				External interrupt mask
EINTPEND	0x560000A8				External interrupt pending
GSTATUS0	0x560000AC			R	External pin status
GSTATUS1	0x560000B0			R/W	Chip ID
GSTATUS2	0x560000B4				Reset status
GSTATUS3	0x560000B8				Inform register
GSTATUS4	0x560000BC				Inform register
MSLCON	0x560000CC				Memory sleep control register
RTC					
RTCCON	0x57000043	0x57000040	B	R/W	RTC control
TICNT	0x57000047	0x57000044			Tick time count
RTCALM	0x57000053	0x57000050			RTC alarm control
ALMSEC	0x57000057	0x57000054			Alarm second
ALMMIN	0x5700005B	0x57000058			Alarm minute
ALMHOUR	0x5700005F	0x5700005C			Alarm hour
ALMDATE	0x57000063	0x57000060			alarm day
ALMMON	0x57000067	0x57000064			Alarm month
ALMYEAR	0x5700006B	0x57000068			Alarm year
BCDSEC	0x57000073	0x57000070			BCD second
BCDMIN	0x57000077	0x57000074			BCD minute
BCDHOUR	0x5700007B	0x57000078			BCD hour
BCDDATE	0x5700007F	0x5700007C			BCD day
BCDDAY	0x57000083	0x57000080			BCD date
BCDMON	0x57000087	0x57000084			BCD month
BCDYEAR	0x5700008B	0x57000088			BCD year

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表 1-4 。 s3c2440a 特殊寄存器（表 13/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
A/D Converter					
ADCCON	0x58000000	←	W	R/W	ADC control
ADCTSC	0x58000004				ADC touch screen control
ADCDLY	0x58000008				ADC start or interval delay
ADCDAT0	0x5800000C			R	ADC conversion data
ADCDAT1	0x58000010				ADC conversion data
ADCUPDN	0x58000014			R/W	Stylus up or down interrupt status
SPI					
SPCON0,1	0x59000000,20	←	W	R/W	SPI control
SPSTA0,1	0x59000004,24			R	SPI status
SPPIN0,1	0x59000008,28			R/W	SPI pin control
SPPRE0,1	0x5900000C,2C				SPI baud rate prescaler
SPTDAT0,1	0x59000010,30				SPI Tx data
SPRDAT0,1	0x59000014,34			R	SPI Rx data
SD Interface					
SDICON	0x5A000000	←	W	R/W	SDI control
SDIPRE	0x5A000004				SDI baud rate prescaler
SDICARG	0x5A000008				SDI command argument
SDICCON	0x5A00000C				SDI command control
SDICSTA	0x5A000010			R/(C)	SDI command status
SDIRSP0	0x5A000014			R	SDI response
SDIRSP1	0x5A000018				SDI response
SDIRSP2	0x5A00001C				SDI response
SDIRSP3	0x5A000020				SDI response
SDIDTIMER	0x5A000024			R/W	SDI data / busy timer
SDIBSIZE	0x5A000028				SDI block size
SDIDCON	0x5A00002C				SDI data control
SDIDCNT	0x5A000030			R	SDI data remain counter
SDIDSTA	0x5A000034			R/(C)	SDI data status
SDIFSTA	0x5A000038			R	SDI FIFO status
SDIIMSK	0x5A00003C	←	W		SDI interrupt mask
SDIDAT	0x5A000043	0x5A000040	B	R/W	SDI data

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表 1-4 。 s3c2440a 特殊寄存器（表 14/14 ）

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
AC97 Audio-CODEC Interface					
AC_GLBCTRL	0x5B000000	←	W	R/W	AC97 global control register
AC_GLBSTAT	0x5B000004			R	AC97 global status register
AC_CODEC_CMD	0x5B000008			R/W	AC97 codec command register
AC_CODEC_STAT	0x5B00000C			R	AC97 codec status register
AC_PCMADDR	0x5B000010				AC97 PCM out/in channel FIFO address register
AC_MICADDR	0x5B000014				AC97 mic in channel FIFO address register
AC_PCMDATA	0x5B000018			R/W	AC97 PCM out/in channel FIFO data register
AC_MICDATA	0x5B00001C				AC97 MIC in channel FIFO data register

S3C2440A专用寄存器注释：

1．在小端模式下，必须使用小端地址；大端模式下，必须使用大端地址；

2．每个特殊寄存器必须按照推荐的方式进行操作；

3．除了ADC寄存器，RTC寄存器和UART寄存器外，其他寄存器都必须以字为单元（32位）进行读写。

4．对ADC,RTC,UART寄存器进行读/写时，必须仔细考虑使用的大/小端模式。

5．W ：32位寄存器，必须用LDR/STR指令或整型数型指针(int *)进行访问；

HW：16位寄存器，必须用LDRH/STRH或短整型数指针(short int *)访问；

B ：8位寄存器，必须用LDRB/STRB或字符型指针(char int *)访问。

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